# Exhibit 31

PERICOM®

Application Note 41

# *A Closer Look at LVDS Technology*

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## Introduction

With the increase in demand for high throughputs, current technologies are becoming less efficient. Data transmission devices like RS-422, RS-485, SCSI and other devices are limited in data rate and power dissipation. With LVDS, data rate has increased tremendously to meet the demand in the high bandwidth market and yet still consumes less power than many current devices. LVDS offers low-power, low-noise coupling, low EMI emissions, and switching capability beyond many current standards. LVDS applications can be used anywhere where high data rate is required and needed to be transfer over a distance. LVDS technology can be found in printers, flat panels, switches, routers, audio/video digital signal processing and many more other applications. In this application note, it will provide a general overview of LVDS technology.

## *What is LVDS?*

LVDS stands for Low Voltage Differential Signaling. LVDS is defined in the TIA/EIA-644 standards and the IEEE 1596.3 standards. The TIA/EIA-644 standards specified the driver's output and the receiver's input, while the IEEE 1596.3 standards defined the signaling level of LVDS. LVDS features low voltage swing with differential constant current source scheme capable of reaching a maximum recommended data rate of 655Mbps. The theoretical values can reach a maximum rate of 1.923Gbps. It should be noted that the maximum data rate is application specific as well as device specific. LVDS technology can be used with distance ranging from a few inches to 10 meters. Again, noted that the operating distance is also applications and device specific. Standard LVDS are primary designed for point-to-point applications where as, Bus LVDS (BLVDS) was defined to support multi-point applications. Figure 1 shows a generic LVDS point-to-point configuration.

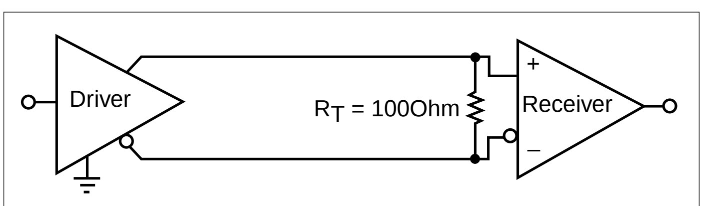


*Figure 1. LVDS Circuit*

## *Low Voltage*

LVDS voltage swing is the lowest compare RS-422, RS-485, SCSI or any other current devices by today's standards. LVDS voltage swing range from 250mV(minimum) to 450mV (maximum) with a typical value of 350mV. Because the voltage swing is very low and will require less time to rise and fall, it is able to achieve higher operating frequency than CMOS and TTL with the same slew rate. It has an offset voltage of 1.2V above ground. Because its operating voltage is centered around 1.2V with respect to the driver's ground, LVDS does not depend on a specific power supply such as 5V or 3.3V making it easy for LVDS to migrate to new low supply voltage technology. Since it is centered around 1.2V, it is also less susceptible to noise since noise often occurs at Vcc or Ground. Low power consumption and lower current is also another result from the low voltage swing. EMI levels are much less than traditional CMOS, TTL, or even PECL. The low EMI emissions are also due to the use of differential transmission.

## *Differential Signaling*

The communication between the driver and the receiver are done through differential signaling. Differential signaling offers enormous advantages over single-ended technologies because it is less susceptible to noise. In using differential signaling, two-balanced signals are transmitted through the line in opposite direction. Because the signals are of the same magnitude but with opposite direction, the electromagnetic field from the two signals are radiated in opposite direction. As a result, they cancel out most of each other EMI. Figure 2 shows the EMI cancellation effect. Figure 2a, shows a single-ended signal with EMI radiating in only one direction. Figure2b shows a differential signal, with EMI radiating in opposite direction thereby canceling out most of the EMI.

Differential signaling also offers what is known as common-mode rejection at the LVDS receiver's end, which works similar to the EMI canceling effect. The advantage of common-mode rejection is that the receiver will ignore any noise that is coupled equally on the differential signals and only consider the differences between the two signals. Unlike single-ended signal where common-mode rejections are not found, noise on the line may cause the device to trigger unintentionally. Figure 3a shows a single-ended signal. Figure 3b shows a differential signal with common mode rejection. In Figure 3b, the receiver will only consider the 350mV swing differences.

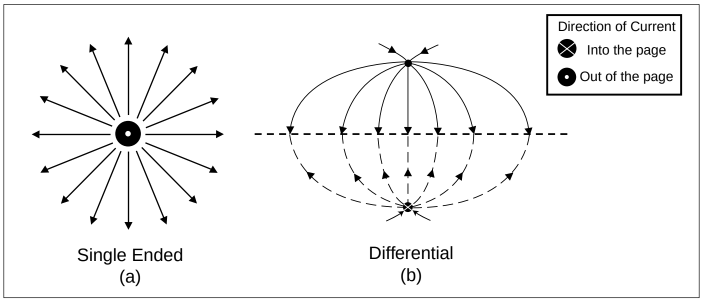


*Figure 2. EMI for Single-ended signal and Differential Signal*

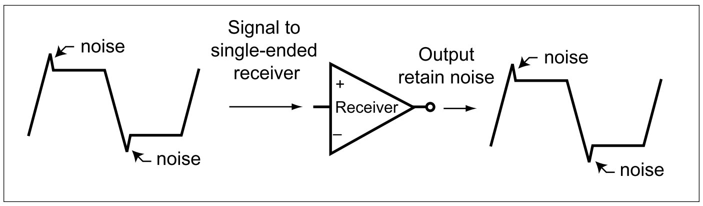


*Figure 3a. Noisy input signal to a signal-ended receiver will not eliminate the noise*

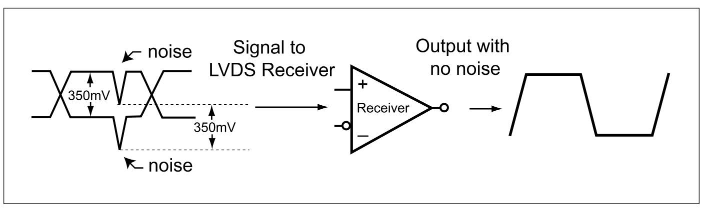


*Figure 3b. Differential signals with common-mode rejection at the LVDS receiver. The receiver will only consider the difference between the two signals.*

## *Failsafe*

LVDS technology also incorporates a failsafe feature at the receiver's end to force a logic HIGH in an event that an undetermined logic state occurs. The failsafe features are enabled under three conditions: open circuit, short circuit, and terminate circuit. Open condition occurs when the input pins at the receiver's end, that are not in use, are left floating. In an open condition, the output would be forced to a logic HIGH. Without the failsafe feature, pins that are left floating will be able to pick up noise thereby possible giving fault data. For shorted condition, failsafe would also forced a logic HIGH at the output. For terminated condition, if the drive is powered off or is removed from the line, it would also force a logic HIGH at the output. Figure 4a, 4b, and 4c illustrate the three conditions the failsafe features would be enabled.

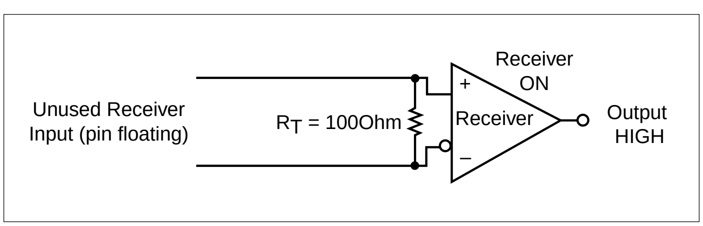


*Figure 4a. Failsafe Open Condition*

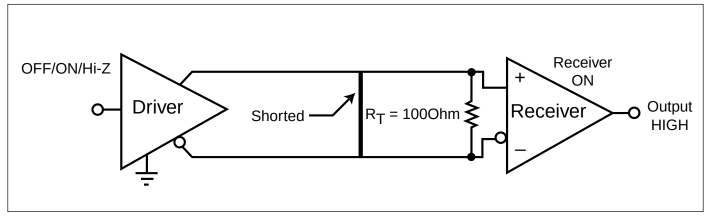


*Figure 4b. Failsafe Shorted Condition*

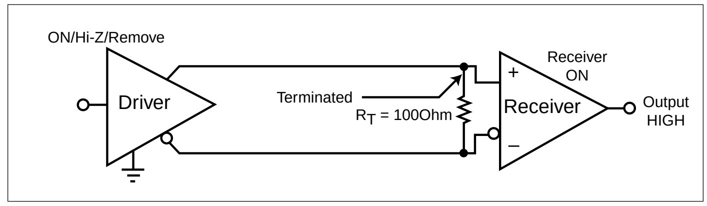


*Figure 4c. Failsafe Terminated Condition*

## *Termination*

LVDS requires a termination resistor in order to generated a Differential Output Voltage ($V_{OD}$) across the resistive termination load at the receiver's input. A termination resistor is also required because a current loop of 2.5mA to 4.5mA is needed. LVDS technology operates at sub-nanoseconds level so proper termination is required to obtain good signal qualities and retained minimal reflections. The termination resistor is required because at such high bandwidth, LVDS transmission media such as cable or PCB trace can no longer be treated a simple wire or trace, but as a transmission-line media. An important factor associated with transmission line is that it must be terminated and the termination must matched the characteristic impedance of the PCB trace to prevent reflections from occurring. The characteristic impedance should be matched with a termination resistor of approximately 100Ω and should be placed as close as possible to the input of the receiver. With proper termination, not only reflections are minimal, but also electromagnetic emissions can be reduced. Some LVDS products have embedded termination resistors. It should be noted that proper termination is mandatory for good signal quality, but trace length should also be minimal and have equivalent length to have optimal signal quality.

## *LVDS vs. PECL*

How does LVDS compare to PECL? LVDS and PECL are both capable of high data rate. But with PECL, the power consumption is much greater compared to LVDS. PECL can have as much as 90% more power consumption than LVDS. LVDS is also capable of operating at a low voltage swing of only ±350mV where as PECL has a voltage swing of ±800mV. Figure 4 compares the voltage swing signals between LVDS and PECL. LVDS also benefits over PECL because it does not depend on a specific power supply such as 5V or 3.3V making it easy to migrate to new low power supply technologies than PECL. LVDS technology also has a more simplified termination layout compared to PECL. LVDS requires only one 100Ω termination resistor place at the input of the receiver. Unlike LVDS, PECL requires a more complex termination scheme. Two 220Ω pull-down resistors

are required at the output of the driver as well a 100Ω resistor at the input of the receiver. Figure 6 shows the termination scheme comparison between LVDS and PECL. Table 1 shows a comparison with LVDS and PECL as well as other standards.

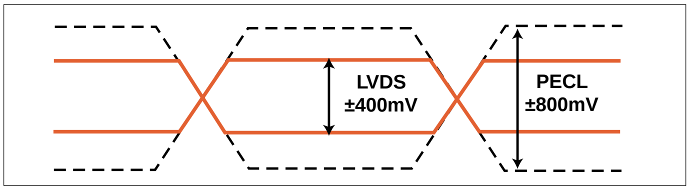


***Figure 5.*** **PECL and LVDS Voltage Swing Comparision**

## *Conclusion*

LVDS technology is currently one of the fastest low power data transmission available. As the demand for higher data rate increases, LVDS will becomes more crucial. LVDS will become more vital to the solution of new technology such as Hyper Transport whose core technology is based on LVDS technology. Pericom Semiconductor offers a variety of LVDS products, including BUS LVDS and LVDS products with embedded termination resistor.

| Parameter | TTL/CM-OS | GTL/BTL | RS-422 | PECL | LVDS |
|---|---|---|---|---|---|
| Signalling | Single Ended | Single \Ended | Differential | Differential Single Ended | Differential |
| Output Voltage Swing | 2.4V - 5.5V | 2.4V - 5.5V | ±2V | ±800mV | ±350mV |
| Reciever Threshold | 1.2V - 1.5V | 1.2V | ±200mV | ±200mV | ±100mV |
| Maximum Speed | <100Mbps | <100Mbps | >10Mbps | >400Mbps | >400Mb-ps |
| Drive Current | 75mA | 40mA-80-mA | 150mA | 40mA-60m-A | 3mA-10-mA |
| Noise generation | High | Medium | Low | Medium | Low |
| Power Dissipation | High | Medium - High | Low | Medium | Very Low |

***Table 1. Comparison between LVDS and Other Standards***

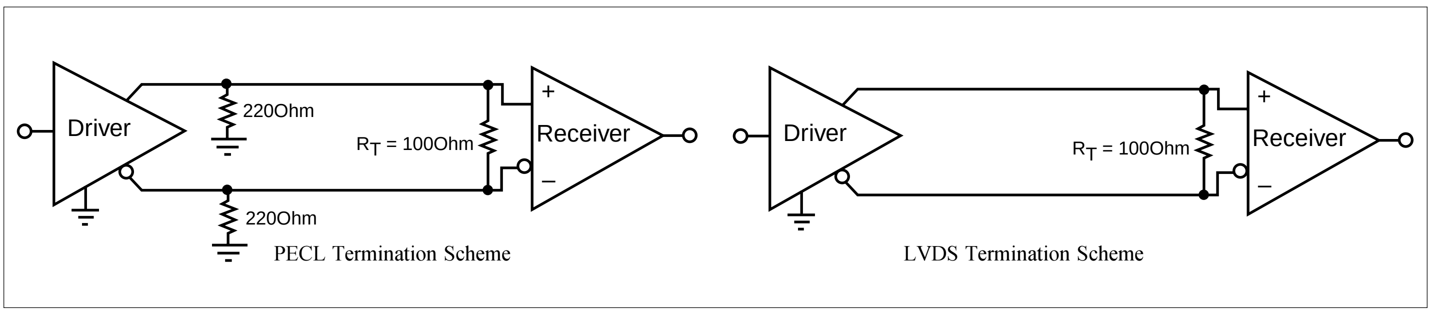


***Figure 6. Termination Scheme for PECL and LVDS***

## *LVDS Advantages*

- high data rate (1.923Gbps maximum)
- does not depend on a specific power supply
- low power
- low cost
- low EMI (noise)

## *Glossary*

LVDS – Low Voltage Differential Signaling

RS-422 – EIA serial transmission standard that extends transmis sion speeds and distances beyond those of RS-232, RS-423 is an unbalanced system; RS-422 is a balanced system with a higher level of \ noise immunity. (RS-422)-Electrical characteristics of balanced-voltage digital interface circuits.

RS-423 – Electrical characteristics of unbalanced-voltage for digital interface circuits

RS-485 – EIA serial interface standard for multi-point lines

PECL – Positive Emitter Couple Logic

SCSI – Small Computer System Interface
A peripheral I/O interface with a standard independent protocol that allows many different
peripheral devices to be attached to the host's SCSI port

EMI – Electromagnetic Interference

IEEE – Institute of Electrical and Electronics Engineering

TIA/EIA-644 – Telecommunications Industry Association/Electronic Industries Association

**Reference:**

1. TIA/EIA-644 Standards
2. IEEE 1596.3 Standards
3. Stephen Kempainen and John Goldie "Low-Voltage Signaling Yields Megatransfers Per Second with Milliwatts of Power", EDN Sept. 1996